IOSR Journal of Engineering (IOSRJEN)
e-ISSN: 2250-3021, **p**-ISSN: 2278-8719
Vol. 3, Issue 5 (May 2013), ||V1 || PP 11-17

Low Power and High Fault Coverage BIST TPG

K.Vasudevareddy[1] K.V.Ramanaiah[2] ` K.Sravani[3]
Asst.Proff NBKRIST Vidyanagar
Associate Professor YVU Proddatur
Asst.Proff NBKRIST Vidyanagar

Abstract: This paper presents a low hardware overhead test pattern generator (TPG) for scan-based Built-In Self-Test (BIST) that can reduce switching activity in circuits under test (CUTs) during BIST and also achieve very high fault coverage with reasonable lengths of test sequences. The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-weight WRBIST. Test patterns generated by the LT-RTPG detect easy-to-detect faults and test patterns generated by the 3-weight WRBIST detect faults that remain undetected after LT-RTPG patterns are applied. The proposed BIST TPG does not require modification of mission logics, which can lead to performance degradation. Experimental results for ISCAS'85 benchmark circuits demonstrate that the proposed BIST can significantly reduce switching activity during BIST while achieving 100% fault coverage for all ISCAS'85 benchmark circuits. Larger reduction in switching activity is achieved in large circuits. Experimental results also show that the proposed BIST can be implemented with low area overhead.

IndexTerms: *Built-in self-test (BIST), heat dissipation during test application, low power testing, power dissipation during test application, random pattern testing.*

I. INTRODUCTION

SINCE in built-in self-test (BIST), test patterns are generatedand applied to the circuit-under-test (CUT) by on-chiphardware, minimizing hardware overhead is a major concernof BIST implementation. Unlike stored pattern BIST, whichrequires high hardware overhead due to memory devices requiredto store precomputed test patterns, pseudorandom BIST,where test patterns are generated by pseudorandom patterngenerators such as linear feedback shift registers (LFSRs) andcellular automata (CA), requires very little hardware overhead.However, achieving high fault coverage for CUTs that containmany random pattern resistant faults (RPRFs) only with(pseudo) random patterns generated by an LFSR or CA oftenrequires unacceptably long test sequences thereby resulting inprohibitively long test time. The random pattern test lengthrequired to achieve high fault coverage is often determined by only a few RPRFs .Several techniques have been proposed to address thisproblem. Reseedable and/or reconfigurable LFSRs are random patterns that do notdetect any new faults are mapped into deterministic tests forRPRFs. In test point insertion (TPI) techniques ,controland observation points are inserted at selected gates to improvedetection probabilities of RPRFs. In weighted random pattern ,testing the outputs of test pattern generator (TPG)are biased to generate test sequences that have nonuniformsignal probabilities to increase detection probabilities of RPRFsthat escape pseudorandom test sequences, which have a uniformsignal probability of 0.5. Random pattern generatorsuse Markov sources to exploit spatialcorrelation between state inputs that are consecutively locatedin the scan chain. A 3-weight weighted random BIST (3-weightWRBIST) can be classified as an extreme case of conventionalweighted random pattern testing BIST. However, in contrastto conventional weighted random pattern testing BIST wherevarious weights, e.g., 0, 0.25, 0.5, 0.75, 1.0, can be assignedto outputs of TPGs, in 3-weight WRBIST, only three weights,0, 0.5, and 1, are assigned. Since only three weights are used,circuitry to generate weights is simple; weight 1 (0) is obtainedby fixing a signal to a 1 (0) and weight 0.5 by driving a signalby an output of a pseudorandom pattern generator, such as anLFSR. Weight sets are calculated from test cubes for RPRFs.Though the attainment of high fault coverage with practicallengths of test sequences is still one major concern of BISTtechniques, reducing switching activity has become another importantobjective. It has been observed that switching activityduring test application is often significantly higher than thatduring normal operation .The correlation between consecutiverandom patterns generated by an LFSR is low—this is awell-known property of LFSR generated patterns. Onthe other hand, significant correlation exists between consecutivepatterns during the normal operation of a circuit. Hence,switching activity in a circuit can be significantly higher duringBIST than that during its normal operation. Finite-state machinesare often implemented in such a manner that vectorsrepresenting successive states are highly correlated to reduce power dissipation . However, use of design-for-testability(DFT) techniques such as scan significantly decreases the correlationbetween consecutive state

vectors. Use of scan allows toapply patterns that cannot appear during normal operation to thestate inputs of the CUT during test application. Furthermore, thevalues applied at the state inputs of the CUT during scan shiftoperations represent shifted values of test vectors and circuit responsesand have no particular temporal correlation. Excessiveswitching activity due to low correlation between consecutivetest patterns can cause several problems.Since heat dissipation in a CMOS circuit is proportional toswitching activity, a CUT can be permanently damaged dueto excessive heat dissipation if switching activity in the circuitduring test application is much higher than that during its normaloperation. Heat dissipated during test application is already influencingthe design of test methodologies for practical circuits.

II. 3-WEIGHT WRBIST

A. GENERATOR

In this paper, we assume that the Combinational CUT has primary and state inputs, and employs full-scan. Even though the proposed BIST TPG is applicable to scan designs with multiple scan chains, we assume that all primary and state inputs are driven by a single scan chain unless stated otherwise (application to multiple scan chains is discussed separately) only for clarity and convenience of illustration. A *test cube* is a test pattern that has unspecified inputs. The *detection probability* of a fault is defined as the probability that a randomly generated test pattern detects the fault. In the 3-weight WRBIST scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs; the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF.

B. MINIMIZING SWITCHING ACTIVITY DURING BIST

The BIST TPG proposed in this paper reduces switching activity in the CUT during BIST by reducing the number of transitions at scan inputs during scan shift cycles. In this paper, we assume that the sequential CUT is implemented in CMOS, and employs full-scan. If scan input p_i is assigned v_j, where $v \in \{0,1\}$,at time $t-1$ and assigned the opposite value at time t_j, then a transition occurs at p_i at time t_j. The transition that occurs at scan input p_i can propagate into internal circuit lines causing more transitions. During scan shift cycles, the response to the previous scan test pattern is also scanned out of the scan chain. Hence, transitions at scan inputs can be caused by both test patterns and responses. Since it is very difficult to generate test patterns by a random pattern generator that cause minimal number of transitions while they are scanned into the scan chain and whose responses also cause minimal number of transitions while they are scanned out of the scan chain, we focus on minimizing the number of transitions caused only by test patterns that are scanned in. Even though we focus on minimizing the number of transitions caused only by test patterns, our extensive experiments show that the proposed TPG can still reduce switching activity significantly during BIST .Since circuit responses typically have higher correlation among neighbourhood scan outputs than test patterns, responses cause fewer transitions than test patterns while being scanned out.

A transition at the input of the scan chain at scan shift cycle t_j, which is caused by scanning in a value that is opposite to the value that was scanned in at the previous scan shift cycle $t-1$, continuously causes transitions at scan inputs while the value travels through the scan chain for the following scan shift cycles. Fig. 5 describes scanning a scan test pattern 01100 into a scan chain that has five scan flip-flops. Since a 0 is scanned into the scan chain at time t_j=0, the 1 that is scanned into the scan chain at time t_j=1 causes a transition at the input of the scan chain and continuously causes transitions at the scan flip-flops it passes through until it arrives at its final destination p_i at time t_j=5. In contrast, the 1 that is scanned into the scan chain at the next cycle t_j=2 causes no transition at the input of the scan

chain and arrives at its final destination p_2 at time t_j=5 without causing any transition at the scan flip-flops it passes through. This shows that transitions that occur in the entire scan chain can be reduced by reducing transitions at the input of the scan chain. Since transitions at scan inputs propagate into internal circuit lines causing more transitions, reducing transitions at the input of scan chain can eventually reduce switching activity in the entire circuit.

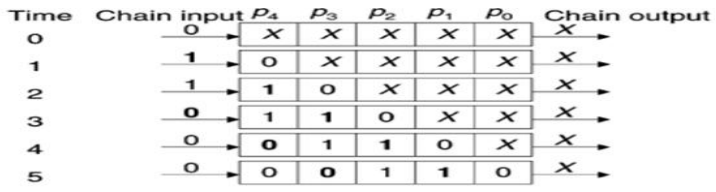

Fig. 5. Transitions at scan chain input.

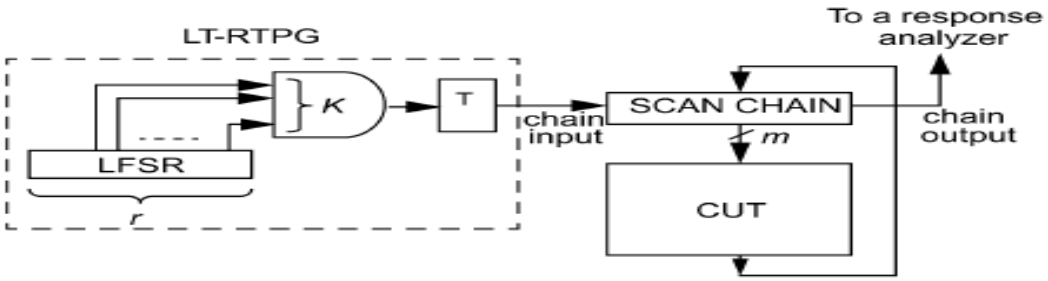

Fig. 6. LT-RTPG.

In 3-Weighted Random Built-In-Self Test, the combinational CUT has 'm' primary and state inputs, and employs full-scan. Even though the implemented BIST TPG is applicable to scan designs with multiple scan chains, the all primary and state inputs are driven by a single scan chain unless stated otherwise (application to multiple scan chains) only for clarity and convenience of illustration. A test cubeis a test pattern that has unspecified inputs. The detection probabilityof a fault is defined as the probability that a randomly generated test pattern detects the fault. In the 3-weight WRBIST scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs, the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF. A generator or weight setis a vector that represents weights that are assigned to inputs of the circuit during 3-weight WRBIST. Inputs that are assigned weight 1(0) are fixed to 1(0) and inputs that are assigned weight 0.5 are driven by outputs of the pseudorandom pattern generator, such as an LFSR and a CA. A generator is calculated from a set of deterministic test cubes for RPRF's.

Pseudo-random pattern sequences generated by an LFSR and a CA are modified (fixed) by controlling the AND and OR gates with overriding signals S0 and S1, fixing a random value to a '0' is achieved by setting 'S0' to a '1' and 'S1' to a' 0' and fixing a random value to a '1' is achieved by setting 'S1' to a '1'. Overriding signals 'S0' and 'S1' are driven by the outputs of T flip-flops,TF0 and TF1 .The inputs of TF0 and TF1 are in turn driven by the outputs of the decoding logic 'D0' and 'D1' respectively, which are generated by the outputs of the shift counter and the generator counter as inputs.

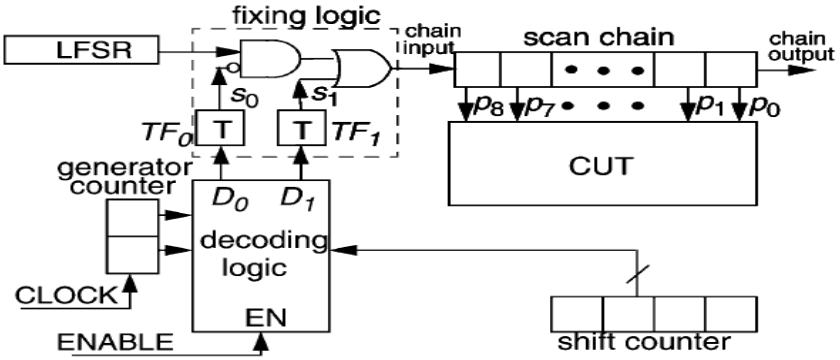

Figure 6: 3-Weight Weighted Random BIST

Hence, hardware overhead for implementing a 3-weight WRBIST is incurred only by the decoding logic and the fixing logic, which includes two toggle flip-flops, an AND and an OR gate. Since the fixing logic can be implemented with very little hardware, overall hardware overhead for implementing the serial fixing 3-weight WRBIST is determined by hardware overhead for the decoding logic.

III. LT-RTPG USING BASIC LINEAR FEEDBACK SHIFT REGISTER (LFSR)

The Low Transition Random Test Pattern Generator (LT-RTPG) reduces switching activity during BIST by reducing transitions at scan inputs during scan shift operation. The LT-RTPG is comprised of an r-stage LFSR, a K-input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware. Each of 'K' inputs of the AND gate is connected to either a normal or an inverting output of the LFSR stages. If large K is used, large sets of neighboring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. In this work, LT-RTPGs with only K=2 or 3 are used since a T- flip-flop holds previous values until the input of the T flip-flop is assigned a 1,the same value 'v', where v E{0,1}, is repeatedly scanned into the scan chain until the value at the output of the AND gate. Hence, adjacent scan flip-flops are assigned identical values in most test patterns

and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations. The LT-RTPG can reduce heat dissipation during overall scan testing. LT-RTPG detects Easy-to- detect faults, those faults are left over by LT-RTPG, are called Random Pattern Resistant Faults (RPRF).

It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from a parent test vector. These observations are exploited and improve fault coverage for circuits that have large numbers of RPRFs. I have also observed that tests for faults that escape LT-RTPG test sequences share many common input assignments.

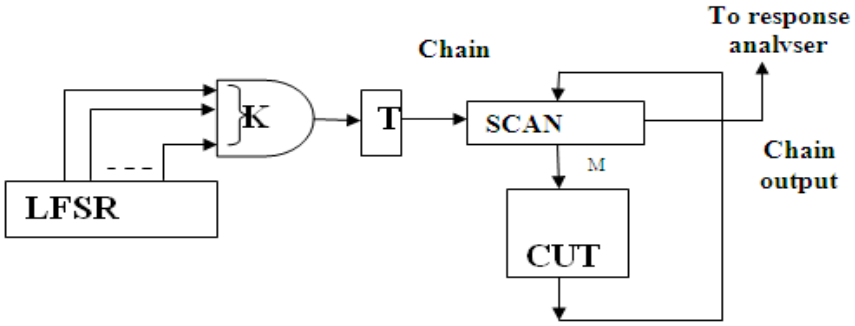

Figure 6.1: LT-RTPG using basic LFSR

This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits.

IV. PROPOSED TEST PATTERN GENERATOR

The proposed BIST is comprised of two TPGs: an LT-RTPG and a 3-weight WRBIST (see Fig. 7). The multiplexer, which drives the input of scan chain, selects a test pattern source between the LT-RTPG and the 3-weight WRBIST.

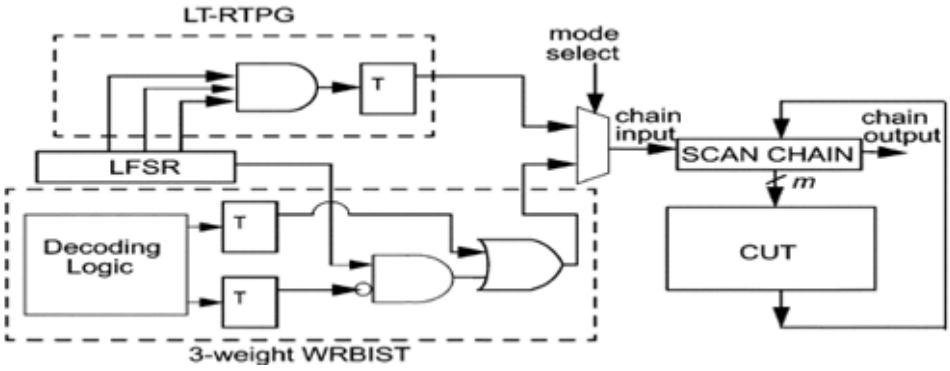

Fig. 7. Proposed BIST TPG.

In the first test session, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults. In the second session, test patterns that are generated by the 3-weight WRBIST are selected to detect the faults that remain undetected after the first session. Considering the fact that an LT-RTPG can be implemented with very little hardware overhead (only one flip-flop and one AND gate in addition to an LFSR), overall hardware overhead to implement the proposed TPG is determined by hardware overhead for the decoding logicof the 3-weight WRBIST.

V. SIMULATION RESULTS:

5.1 Test pattern of C17 circuit:

In the below simulation window, Fig 7.3 C17 circuit predefined test pattern output, The clock frequency is set to 10MHz.In order get random pattern resistant faults I need to have predefined test patterns of faulty C17 circuit. Normally 4 faults have been inserted into C17 circuit. The different test patterns generated by the LFSR are applied to C17 circuit then at each and every fault corresponding test vector is noted. These patterns are the pre-defined test vectors of C17 circuit.

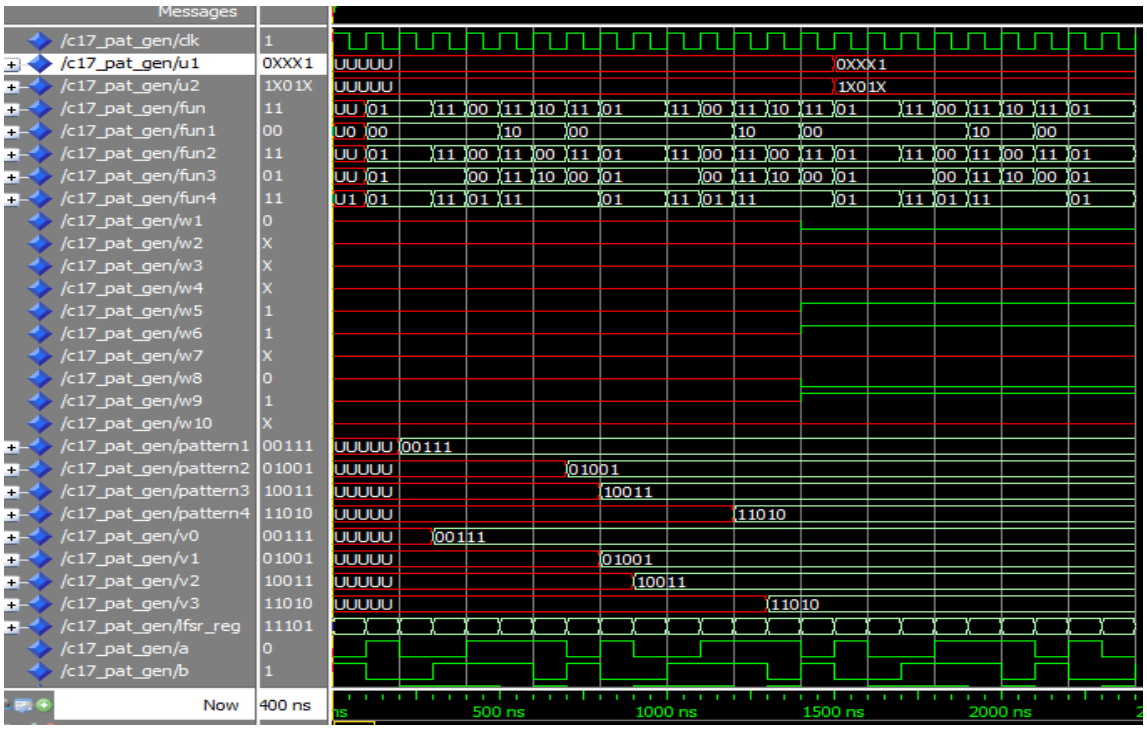

Figure 8.1: C17 circuit predefined test pattern output

5.2 Simulated output of Implemented system

In the below simulation window, Fig 7.4 Complete Implemented system output, the clock frequency is set to 10MHz.Both easy to detect faults and random pattern resistant faults are detected .The fault signal is high ,the value of fault covered as 9. Hence the fault coverage is improved to 25%.

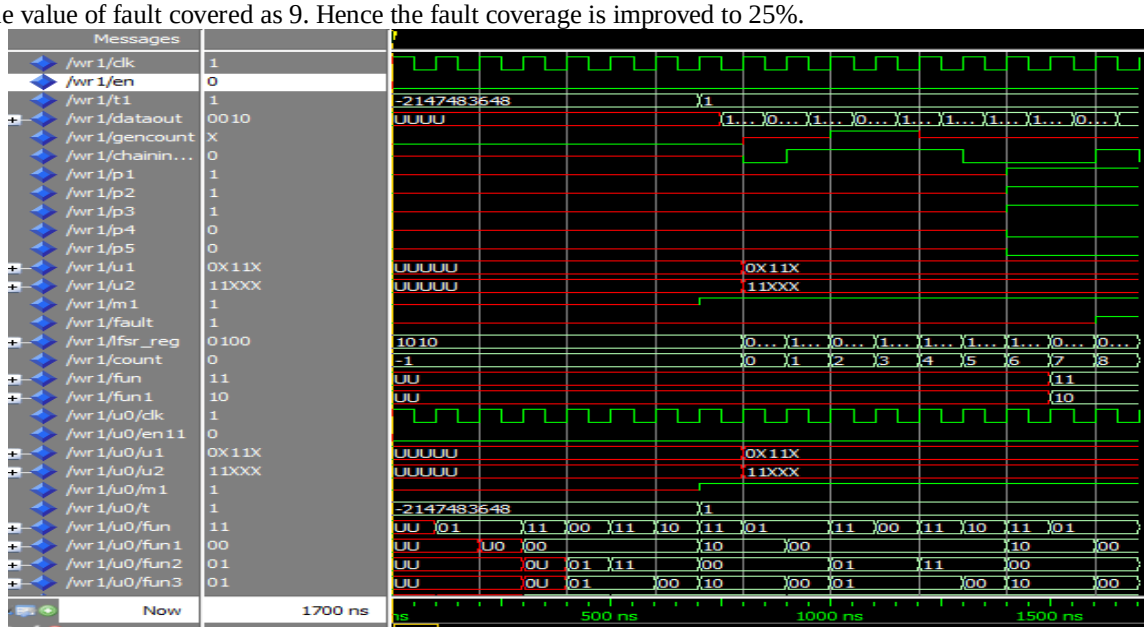

Figure 8.2: Proposed system output

This window consist of LFSR generated patterns which will be labeled as lfsr_reg. After applying C17 circuit predefined patterns 1000,1001 as set, reset values the final fault becomes high ,for 0000,1111 values final fault signal is low. Hence the fault final signal will be high only for the predefined test patterns of C17 circuit

VI. SYNTHESIS RESULTS

6.1 Gate count for implemented system

The below figure shows gate count report for implemented system, Total equivalent gate count for the design is 324.Additional JTAG gate count for IOBs is 912 gates.

ZZ Project Status			
Project File:	zz.ise	**Current State:**	Placed and Routed
Module Name:	exs_cc	**• Errors:**	No Errors
Target Device:	xc2s600e-7fg456	**• Warnings:**	12 Warnings
Product Version:	ISE, 8.1i	**• Updated:**	Fri Jan 4 00:45:19 2013

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	14	13,824	1%	
Number of 4 input LUTs	34	13,824	1%	
Logic Distribution				
Number of occupied Slices	22	6,912	1%	
Number of Slices containing only related logic	22	22	100%	
Number of Slices containing unrelated logic	0	22	0%	
Total Number of 4 input LUTs	34	13,824	1%	
Number of bonded IOBs	18	325	5%	
IOB Flip Flops	1			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	324			
Additional JTAG gate count for IOBs	912			

Figure 7.3: Proposed system synthesis report

7.4.2 Usage of power, voltage and current:

Power summary:	(mA)	P(mW
Total estimated power consumption:		936
Vccint 2.50V:	372	929
Vcco33 3.30V:	2	7
Clocks:	331	826
Inputs:	40	100
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 2.50V:	1	3
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	57C
Ambient temp:	25C
Case temp:	54C
Theta J-A:	34C/W

Figure 7.4: Power consumption analysis report

VII. CONCLUSION

This paper presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in cuts during BIST and also achieve very high fault coverage with a reasonable length of test sequence. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective. Since the correlation between consecutive patterns applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation. Excessive switching activity during test application can cause several problems. The proposed TPG reduces the number of transitions that occur at scan inputs during scan shifting by scanning in the test patterns where neighbouring bits are highly correlated. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-Weight WRBIST. Test sequences generated by the LT-RTPG detect easy-to-detect faults. Faults that escape LT-RTPG test sequences are detected by test patterns generated by the 3-Weight WRBIST.Hardware overhead for the proposed TPG is further reduced by identifying compatible scan chains in multiple scan chain designs.

Experimental results for ISCAS'85 benchmark circuits demonstrate that the proposed BIST can significantly reduce switching activity during BIST while achieving 100% fault coverage for all benchmark circuits. Larger reduction in switching activity is achieved for large circuits, which have long scan chains. The proposed BIST structure does not require modification of mission logic which can cause performance degradation. Experimental results for large industrial circuits demonstrate that the proposed TPG can significantly improve fault coverage of LFSR generated test sequences with low hardware overhead.

REFERENCES:

[1]. Parag K.Lala**"**An Introduction to Logic Circuit Testing", Morgan and Clay Pool Publishers.

[2]. Rolf Isermann," **Fault-Diagnosis Systems-** An Introduction from Fault Detection to Fault Tolerance".

[3]. Muhammad M.Kellah,"Low Power Digital CMOS VLSI circuits and design methodologies".

[4]. H.-C. Tsai, K.-T. Cheng, C.-J. Lin, and S. Bhawmik,Low-Power VLSI Design-An Overview'

[5]. Sung-Mo Kang Yusuf Leblibici,"CMOS Digital Integrated Circuits Analysis and Design"-Third Edition.

[6]. B. Koenemann, "LFSR-Coded Test Patterns for Scan Design", Proc. of EuropeanTest Conference, Munich, Germany, April 1991,pp. 237-242.

[7]. N. Tamarapalli and J. Rajski, "Constructive multi-phase test point in-sertion for scan-based BIST," in Proc. IEEE Int. Test Conf., 1996, pp. 649–658.

[8]. Irith Pomeranz,"3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set for Combinational and Sequential Circuit, "in Proc IEEE vol,.12.no.7 July 2002.

[9]. Seongmoon Wang ,"A BIST TPG for Low PowerDissipation and High Fault Coverage",IEEE transactions on very large scale integration (VLSI) systems, vol. 15, no. 7, July 2007

[10]. S. Wang and S. K. Gupta, "LT-RTPG: A new test-per-scan BIST TPG for low heat dissipation," IEEE Trans. Comput.-Aided Des. Integer. CircuitsSyst., vol. 25, no. 8, pp. 1565–1574, Aug. 2006.